LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A system comprising:

a frequency generator that provides a clock signal having a frequency that varies based on an operating voltage; and

a controller that provides a control signal to adjust the operating voltage based on adjustments to the frequency of the clock signal.

2. (Currently Amended) The system of claim 1, wherein the controller provides the control signal based on a number of cycles for the ~~first~~ clock signal relative to a number of cycles for a second signal over a cycle time that encompasses plural cycles associated with the first and second signals, the second signal having a substantially fixed frequency.

3. (Original) The system of claim 2, wherein the clock signal defines a variable clock signal and the second signal defines a signal having a substantially fixed maximum frequency for the clock signal.

4. (Original) The system of claim 1, further comprising a comparator operative to ascertain an indication of throttle events associated with the frequency generator implementing changes to the frequency of the clock signal, the controller providing the control signal based on the indication of throttle events.

5. (Original) The system of claim 4, wherein the comparator compares the indication of throttle events relative to at least one threshold value to provide a comparator signal that controls adjustments to the reference voltage, the controller providing the control signal based on the comparator signal.

6. (Original) The system of claim 5, wherein the at least one threshold is programmable.

7. (Original) The system of claim 5, wherein the at least one threshold defines at least first and second operating categories, the first operating category corresponding to a condition in which the operating voltage is too low, the second operating condition corresponding to a condition in which operating voltage is too high, the controller providing the control signal to adjust the operating voltage based on a selected one of the first and second operating categories.

8. (Original) The system of claim 7, wherein the at least one threshold further defines a third operating category between the first and second categories in which the operating voltage is sufficiently low and the clock signal is operating within expected operating parameters, the controller preserving the operating voltage when operating in the third category.

9. (Original) The system of claim 4, further comprising first and second counters, the first counter being operative to count a number cycles associated with the clock signal, the second counter being operative to count a number cycles associated with a second signal having a substantially fixed frequency, the comparator ascertaining the indication of throttle events based on the relative number of cycles counted by the first and second counters.

10. (Original) The system of claim 1, further comprising first and second counters, the first counter being operative to count a number cycles associated with the clock signal, the second counter being operative to count a number cycles associated with a second signal having a substantially fixed frequency, the controller providing the control signal based on the relative number of cycles counted by the first and second counters.

11. (Original) The system of claim 10, wherein the relative number of cycles indicated by the first and second counters corresponds to an average indication of a number of changes implemented by the frequency generator to the frequency of the clock signal.

12. (Original) The system of claim 1, further comprising a second frequency generator that provides a second signal having a substantially fixed frequency corresponding to a desired maximum frequency for the clock signal.

13. (Original) The system of claim 1, further comprising:

at least a first path delay network tuned to delay the clock signal to provide a delay signal as a function of the operating voltage, the first path delay emulating operating characteristics of a critical path of an associated integrated circuit;

a comparator associated with the first path delay network, the comparator providing a first comparator signal indicative of desired adjustments to the frequency of the clock signal based on a comparison between the clock signal and the respective delay signal provided by the first path delay network; and

the frequency generator adjusting the frequency of the clock signal based on the first comparator signal.

14. (Original) The system of claim 13, further comprising:

at least a second path delay network tuned to delay the clock signal to provide a second delay signal as a function of the reference voltage, the second path delay network emulating operating characteristics of a critical path of the associated integrated circuit;

a second comparator associated with the second path delay network, the second comparator provides a second comparator signal indicative of desired adjustments to the frequency of the clock signal based on a comparison between the clock signal and each of second delay signal; and

the frequency generator adjusting the frequency of the clock signal based on at least one of the first comparator signal and the second comparator signal.

15. (Original) An integrated circuit comprising the system of claim 1.

16. (Original) A system to adjust voltage, comprising:

means for providing an indication of voltage induced throttle events for an integrated circuit; and

means for controlling a supply voltage of the integrated circuit based on the indication of throttle events.

17. (Original) The system of claim 16, further comprising means for determining a number of cycles for the clock signal relative to a number of cycles for a second signal having a substantially fixed frequency, the determined number of cycles providing an indication of throttle events associated with changes in a frequency of the clock signal.

18. (Original) The system of claim 17, the means for determining further comprising:

means for counting cycles of the clock signal; and

means for counting cycles of the second signal,

the means for controlling adjusting the supply voltage of the integrated circuit based on a relative number of cycles counted by each of the means for counting cycles.

19. (Original) The system of claim 16, further comprising:

means for delaying the clock signal based on the supply voltage to provide a delay signal;

means for comparing the delay signal relative to the clock signal to provide an indication of a level of the supply voltage, and

means for adjusting a frequency of the clock signal based on the indication of the level of the supply voltage provided by the means for comparing.

20. (Original) The system of claim 16, further comprising means for programming at least one threshold value for controlling adjustments to the supply voltage, the means for controlling adjusting the supply voltage based on the indication of throttle events relative to the at least one threshold.

21. (Original) The system of claim 16, wherein the means for controlling implementing control of the supply voltage on a cycle time associated with a power control loop, the cycle time associated with a power control loop being substantially greater than a cycle time associated with the clock signal.

22. (Original) The system of claim 16, wherein the voltage induced throttle invents comprising at least one of adjusting operating frequency of the integrated circuit and implementing stall events relative to the integrated circuit.

23. (Original) A method comprising:

determining whether adjustments to an operating frequency of an integrated circuit are within expected operating parameters based on adjustments made to the operating frequency performed over a cycle time that includes a plurality of cycles at the operating frequency; and

adjusting the supply voltage based on the determination.

24. (Original) The method of claim 23, further comprising adjusting the operating frequency as a function of the supply voltage.

25. (Original) The method of the claim 24, wherein the adjustments to the operating frequency are part of a clock signal control loop having a first cycle time, the adjustments to the supply voltage being part of a power control loop having a second cycle time that is greater than the first cycle time.

26. (Original) The method of claim 25, wherein the second cycle time is more than about one hundred times greater than the first cycle time.

27. (Original) The method of claim 23, further comprising:

counting a number of cycles associated with a first reference signal having a substantially fixed frequency at a maximum operating frequency;

counting a number of cycles associated with a second reference signal provided at the operating frequency that varies based on the supply voltage; and

comparing the number of cycles associated with the first reference signal relative to the number of cycles associated with the second reference signal, the adjustment to the supply voltage being made based on the comparison.

28. (Original) The method of claim 23, further comprising ascertaining an indication of throttle events associated with adjustments to the frequency of the second reference signal based on the comparison, the adjustment to the supply voltage being made based on the indication of throttle events.

29. (Original) The method of claim 28, wherein the adjustment to the supply voltage are made based on comparing the indication of throttle events relative to at least one threshold, the adjustment to the supply voltage being made based on the comparison.

30. (Original) The method of claim 29, further comprising programming the at least one threshold to define operating categories for adjusting the supply voltage.

31. (Original) The method of claim 23, further comprising:

delaying a clock signal by an amount functionally related to the supply voltage to provide a delay signal, the amount of delay corresponding to operating characteristics of a critical path of the integrated circuit; and

adjusting the operating frequency based on a comparison of the delay signal and a clock signal at the operating frequency.